

PATENT ABSTRACTS OF JAPAN

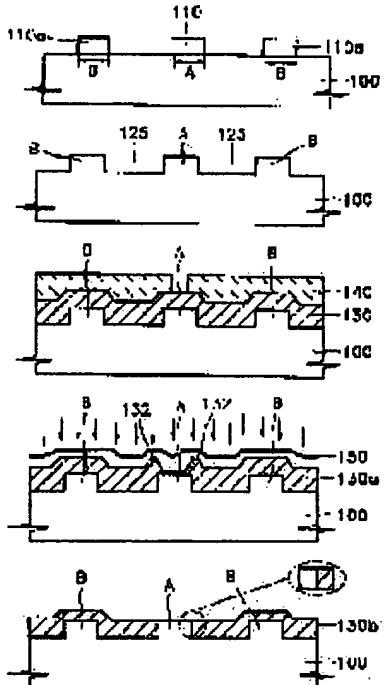
(11)Publication number : **10-022376**
(43)Date of publication of application : **23.01.1998**

(51)Int.CI. **H01L 21/76**
H01L 21/304
H01L 21/66
H01L 27/108
H01L 21/8242

(21)Application number : **08-302981** (71)Applicant : **SAMSUNG ELECTRON CO LTD**
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(30)Priority
Priority number : **96 9623681** Priority date : **25.06.1996** Priority country : **KR**

(54) METHOD FOR ISOLATING SEMICONDUCTOR ELEMENTS



(57)Abstract:

PROBLEM TO BE SOLVED: To accurately evaluate the electric characteristics at a cell array region and peripheral circuit region from evaluated electric characteristics at a TEG region by forming a dummy active region in the TEG region.

SOLUTION: Mask patterns 110, 110a for limiting an active region on a semiconductor substrate 100 in a TEG region and dummy active region B around them and the substrate 100 is etched to form a trench region. An insulation film 130 is formed on the entire surface. A photo resist pattern 140 is formed thereon with leaving the insulation film 130 exposed on the active region A. The exposed insulation film 130 is etched to form an insulation pattern 130a of specified thickness on the active region A. The resist pattern 140 is then removed and the insulation pattern 130a is planarized to form an element isolation film 130b in the trench region 125.

LEGAL STATUS

[Date of request for examination] 14.03.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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